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| 10/712,052 | 11/14/2003 | Yong-Joon Cho | SEC.1063 | 9035 |

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| EXAMINER | |
|---|---|
| UMEZ ERONINI, LYNETTE T | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/712,052 | CHO ET AL. | |
| | Examiner | Art Unit | |
| | Lynette T. Umez-Eronini | 1765 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *6/21/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5,8-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,8-10 and 12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/14/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This communication is in response to Applicants' Remarks in Amendment filed June 21, 2007, which were persuasive in showing the formerly applied references fail to teach wet etching the etch stop layer to remove the etch stop layer over the source region, drain region, and the sidewall spacers. Hence, a new rejection is presented.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US 5,926,710) in view of Sun et al. (US 6,010,931).

Tseng discloses a method of making DRAM cells by forming node contact openings **2** in the second **24** and first insulating **22** layers in a FET (field effect transistor) on a substrate **10**, forming a planar insulating layer **24** over FETs and etching contact openings in each FET (Abstract; column 3, line 52 - column 5, line 40; and **FIG. 2**). The aforementioned reads on,

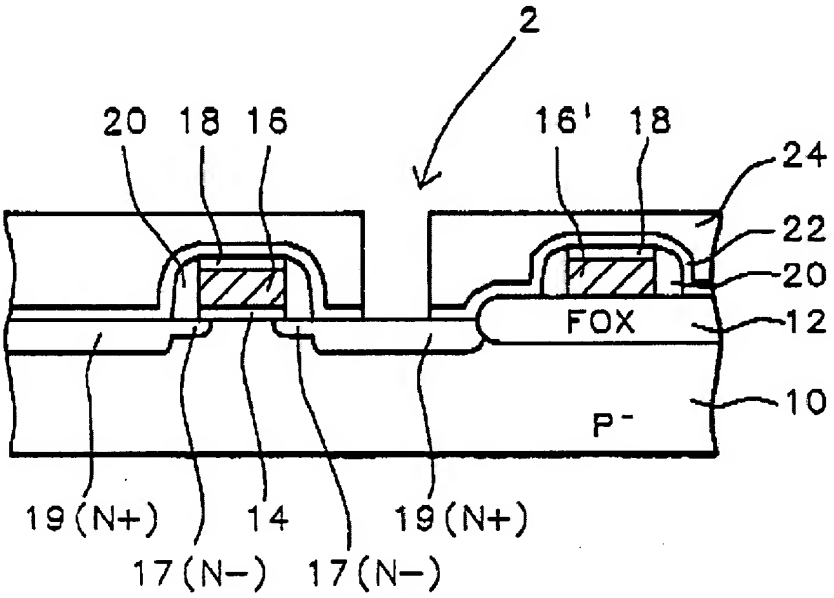


*FIG. 2*

A method for fabricating a semiconductor device, the method comprising:

providing a semiconductor substrate **10** having a device formation region (column 1, lines 7-11 and column 3, lines 52-62); and

forming a gate **14** on the device formation region of the semiconductor substrate **10**, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate

comprises a gate dielectric layer **14**, a gate conductive layer **16** and sidewall spacers **20** located at respective sidewalls of the gate conductive layer **16** (column 1, lines 7-11; column 3, lines 52-62; and column 4, lines 30-44).

Tseng teaches insulating layer **22** (same as Applicant's buffer layer and etch stop layers), composed of a lower $SiO_2$ layer and an upper $Si_3N_4$ layer that is conformally deposited over device areas and field oxide area **12** (column 5, lines 24-27), which reads on,

sequentially forming a buffer layer and an etch stop layer over the source region, the drain region and the gate to obtain an intermediate structure; and forming a buffer layer **22** over the source region **17**, **19**, the drain region **17**, **19** and the sidewall spacers **20** of the gate;

forming an etch stop layer on the buffer layer to obtain an intermediate structure (column 5, lines 24-28); and

forming a planarized first interlayer insulating film **24** over a surface of the intermediate structure (column 5, lines 34-36).

Tseng also teaches performing dry etching process (same as plasma etching) to etch the first insulating layer **24** until the etch stop layer **22** is exposed to form self-aligned contact holes **2** in the first interlayer insulating **24** (column 5, lines 37-41).

Tseng further teaches conventional photolithographic techniques to form node contact openings **2** in the second **24** and first **22** insulating layers to the source/drain contact areas (column 5, lines 36-40).

It is noted, Tseng shows polysilicon layer **26** is deposited over the contact opening **2** before depositing insulating layer **28** over layer **26** (column 5, lines 45-60), which reads on, forming respective contact pads by filling the self-aligned contact hole with conductive polysilicon.

Tseng differs in failing to teach performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively; and

wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers.

Sun illustrates in FIG. **8**, a method of plasma etching (same as dry etching) openings thru dielectric layer **94** to etch stop layer **90** and leaving portions of dielectric layer **96** over other parts of the device (column 8, line - column 9, line 3). One can see the other parts of the device include the sidewall **64**, source/drain regions **80, 82, and 84**, as shown in FIG. **8**. Hence, the aforementioned reads on dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region.

Sun also teaches plasma etching the etch stop layer **90** and alternatively wet etching the etch stop layer from within the openings in the dielectric layer. The latter

etch step reads on wet etching the buffer layer and the etch stop layer. Sun further teaches after the etching steps not only the surfaces of the source, drain regions **80, 84** but also the spacer **64** are exposed (column 9, lines 5-8) which thereby reads on, wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers.

Since the combination of Tseng and Sun uses the same method of etching the same insulation film over an intermediate structure as claimed by Applicants, then using Tseng's etching method in the same manner as in the claimed invention would result the same wherein the first interlayer insulating film has an etching rate slower than the etching rate of the buffer layer relative to a defined dry etching process.

Hence, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Tseng by using Sun's method of etching a self align contact for the purpose of etching without conducting a cleaning step after etching (Sun, column 9, lines 10-13).

4. Claims 1, 2, 5, 10, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view of Sun (US '931) and further in view of Tomita (US 6,806,549 B2).

As to claims 1 and 5, Tseng discloses a method of fabricating a semiconductor device as described above in claim 21 and further discloses

wherein the wet etching of the etch stop layer comprises: removing oxide film remnants on the etch stop layer by wet etching by with an oxide etchant; and removing

the etch stop layer using an oxide etching solution or a nitride etching solution, (column 7, lines 7-11), **in claim 12**; and

wherein the nitride etching solution includes phosphoric acid, $H_3PO_4$ (column 7, lines 7-11), **in claim 14**.

Tseng also teaches wherein the gate **16** is formed to further comprise a hard mask **18** (same as Tseng's cap oxide **18)** on a surface of the gate conductive layer **16** (column 4, lines 54-57), **in claim 2**; and

wherein the etch stop layer **22** is formed of silicon nitride by chemical vapor deposition, (column 5, lines 24-31), **in claim 10**.

Tseng in view of Sun further differ in failing to teach wherein the first interlayer insulating film is silicon oxide film formed by high-density plasma chemical vapor deposition, **in claim 1**.

Tomita discloses, "A silicon oxide film (hereinafter called an "HDP oxide film") formed by means of, e.g., the high-density chemical vapor deposition (HDPCVD) method is taken as the plasma silicon oxide film" (column 4, lines 61-64).

Since Tomita illustrates forming silicon oxide film by HDPCVD) is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ Tomita's method of depositing an oxide layer because such method is used in the manufacturing of semiconductor devices (column 2, lines 59-61).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view of Sun (US '931), and Tomita (US '549 B1) as applied to claim 1 above, and further in view of DeBoer et al. (US 2002/016830 A1).

Tseng in view Tomita and Sun fail to teach wherein the sidewall spacer is formed of silicon nitride by chemical vapor deposition.

DeBoer teaches dielectric spacers may be formed of CVD nitride or oxide layer [0037].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Tseng's oxide spacer with DeBoer's CVD silicon nitride layer, since the oxide and silicon nitride materials of these layers are seen as equivalent because such materials used to form spacers (DeBoer, [0037]).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view Sun (US '931) and Tomita (US '549) as applied to claims 1 and 5 above, and further in view of Hashimoto (US 6,010,955).

Tseng in view Sun and Tomita differs in failing to teach wherein the buffer layer is formed of silicon oxide by thermal oxidation, **in claim 8**.

Hashimoto teaches, " . . .a buffer silicon dioxide layer may be provided before the contact lithography to prevent contact between the resist pattern 150 and substrate 105. In this case, a thin silicon dioxide layer (not shown) having a thickness of about 100 Å is formed by thermal oxidation on diffusion regions 122 of FIG. 3(a) . . . " (column 4, lines 42-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Tseng in view Sun and Tomita by using Hashimoto's buffer layer for the purpose of preventing contact between the substrate and a layer (resist pattern) above the substrate (Hashimoto, column 4, lines 42-47).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view Sun (US '931), Tomita (US '549 B2), and Hashimoto (US 955) as applied to claims 1, 5, and 8 above, and further in view of Lu (US 6,479,341 B1).

Tseng in view of Sun, Tomita, and Hashimoto differ in failing to teach wherein the buffer layer is formed of a mid-temperature oxide (MTO) by low-pressure chemical vapor deposition.

Lu discloses, "A first insulator layer of silicon oxide **9**, is next deposited using LPCVD or PECVD procedures, at a temperature between about 200 to 600 °C" (column 4, lines 16-18), which is formed of the same material, by the same method, and within the same temperature range as Applicants' MTO buffer as specified in the Specification [0020].

Since Lu illustrates forming an oxide layer, which is the same material as Applicants' buffer layer and under the similar conditions as claimed by Applicant, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Tseng in view Sun, Tomita, and Hashimoto by using Lu's method of forming an oxide layer, which is the same as Applicant's MTO buffer because such method is used in forming semiconductor devices (column 2, lines 18-23).

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2), as applied to claims 1 and 12 above and further in view of Chang et al. (US 5,817,562).

Tseng in view of Sun and Tomita differ in failing to teach wherein the oxide etching solution includes a concentration of diluted hydrofluoric acid (HF) having a density of 0.01 wt % through 0.001 wt %.

However, Chang illustrates an oxide etching solution, which includes hydrofluoric acid. (column 6, lines 59-64) is known. Hence it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to select any proportion of wt % of HF in the Chang reference, including the concentration range of wt % of HF as claimed by Applicants, that would effectively accomplish the disclosed composition in the absence of unexpected result because such etchant is used in conventional wet etching to form source/drain contact openings in an oxide **32** layer (Chang, column 6, lines 59-62).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claims 1 and 14 above, and further in view of and Lo (US 5,779,927).

Tseng in view Sun and Tomita differs in failing to teach wherein the concentration of phosphoric acid $H_3PO_4$ is 50 wt % through 80 wt %, **in claim 15**.

Lo teaches and illustrates silicon nitride can be etched at a range of phosphoric acid concentrations between 0 and 95 weight % (column 4, lines 38-43).

Hence it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to select any proportion of wt % of $H_3PO_4$ in the Lo reference, including the concentration range of wt % of $H_3PO_4$ as specifically claimed by Applicant for the purpose of etching at high temperatures (column 2, lines 38-40).

10. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US 710) in view of Sun (US 931), Tomita (US '549 B2) as applied to claims 1 and 5 above, and further in view of Kim et al. (US-PGPUB 2002/0064968 A1).

Tseng in view of Sun and Tomita differs in failing to teach wherein the buffer layer is removed using an etching solution including ammonium hydroxide ($NH_3OH$), hydrogen peroxide ($H_2O_2$), and deionized water, **in claim 16**;

wherein the etching solution includes a concentration of ammonium hydroxide ($NH_4OH$) ranging form about of 0.1 wt % through 1.0 wt %, **in claim 17**;

wherein the etching solution includes a concentration of hydrogen peroxide ($H_2O_2$) ranging form about of 4.0 wt % through 7.0 wt %, **in claim 18**;

wherein the wet etching is performed at a temperature of 30°C through 80°C, **in claim 19**.

Kim teaches wet etching hole spacers formed of a layer of a MTO (which is the same material as applicants' buffer layer) using a mixture of $NH_4OH$ and $H_2O_2$ to remove native oxides formed on the surface of the substrate as well as to remove contaminants remaining in the contact holes ([0030, line 6 - 0031, line 6]). Also since Kim is silent as to the etching temperature, then one can assume that the etching is carried out at standard operating conditions of 25°C and 1 atm.

Since Kim illustrates removing a buffer layer using applicants' specific combination of $NH_4OH$ and $H_2O_2$ is known, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to select any proportion of wt % and temperature in the Kim reference that would effectively accomplish the disclosed

composition in the absence of unexpected results because such etchants are used in removing native oxides and contaminants remaining in contact holes (Kim, [0031]).

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng (US 710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claim 1 above, and further in view of Kim et al. (US 6,342,416 B1).

Tseng in view of Sun and Tomita further differs in failing to teach filling the self-aligned contact holes by depositing the conductive polysilicon over an entirety of the surface of the semiconductor substrate; and

chemical mechanical polishing the conductive polysilicon in the self-aligned contact holes down to a level of an upper portion of the first interlayer insulating film, and **in claim 20**.

Kim teaches polysilicon layer **114** is formed of conductive material, formed on first interlevel dielectric layer **112** including the first contact hole, and is chemically mechanically polished until the top surface of the dielectric layer **112** is exposed to form a bit line contact plug that is connected to the drain and source region of semiconductor substrate (column 3, lines 1-10 and FIG. **1** and **2**).

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Tseng in view of Tomita and Lo by using Kim's method of filling and polishing a conductive material for the purpose of forming a contact plug that is connected to the drain and source region of semiconductor substrate (Kim, column 3, lines 4-10 and FIG. **1** and **2**).

***Response to Arguments***

12. Applicants' arguments, see Remarks, filed 6/21/2007, with respect to the rejection(s) of

claim 21 under 35 U.S.C. 102(b) over U.S. Patent No. 5,926,710 to Tseng;

claims 1, 2, 5, 10, 12, 14, and 15 under 35 U.S.C. 103(a) over Tseng in view of U.S. Patent No. 6,806,549 to Tomita and in view of U.S. Patent No. 5,779,927 to Lo;

claim 3 under 35 U.S.C. 103(a) over Tseng in view of Tomita, Lo, and U.S. Patent Pub. No. 2002/0168830 to DeBoer et al.;

claim 8 under 35 U.S.C. 103(a) over Tseng in view of Tomita, Lo, and U.S. Patent No. 6,010,955 to Hashimoto;

claim 9 under 35 U.S.C. 103(a) over Tseng in view of Tomita, Hashimoto, and U.S. Patent No. 6,479,341 to Lu;

claims 16-19 were rejected under 35 U.S.C. 103(a) over Tseng in view of Tomita and U.S. Patent No. 6,342,416 to Kim et al.; and

claim 20 was rejected under 35 U.S.C.103(a) over Tseng in view of Tomita, Lo, and Kim et al. have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made under 35 U.S.C. 103 (a) on

Claim 21 over Tseng (US 5,926,710) in view of Sun et al. (US 6,010,931);

Claims 1, 2, 5, 10, 12, and 14 over Tseng (US '710) in view of Sun (US '931) and Tomita (US 6,806,549 B2);

Claim 3 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claim 1 above, and further in view of DeBoer et al. (US 2002/016830 A1);

Claim 8 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claims 1 and 5 above, and further in view of Hashimoto (US 6,010,955);

Claim 9 over Tseng (US '710) in view of Sun (US '931), Tomita (US '549 B2) and Hashimoto (US '955) as applied to claims 1, 5, and 8 above, and further in view of Lu (US 6,479,341 B1);

Claim 13 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claims 1 and 12 above, and further in view of Chang et al. (US 5,817,562);

Claim 15 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claims 1 and 14 above, and further in view of Lo (US 5,779,927).

Claims 16-19 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claims 1 and 5 above, and further in view of Kim et al. (US-PGPUB 2002/0064968 A1); and

Claim 20 over Tseng (US '710) in view of Sun (US '931) and Tomita (US '549 B2) as applied to claim 1 above, and further in view of Kim et al. (US 6,342,416 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

ltue

August 29, 2007

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER